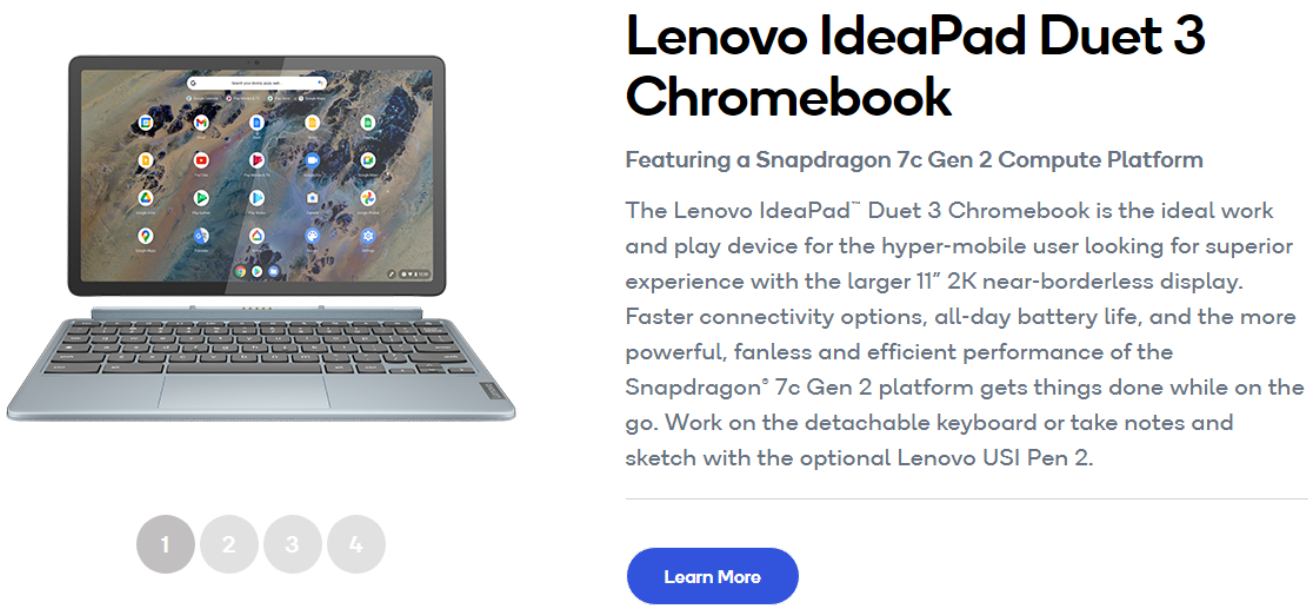
EXHIBIT 030

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
1. An integrated circuit comprising:	Without conceding that the preamble of claim 1 of the '2893 Patent is limiting, the Lenovo IdeaPad Duet 3 Chromebook (hereinafter, the "Lenovo product") includes an integrated circuit. For example, the Lenovo product includes the Qualcomm Snapdragon 7c Gen 2 Compute Platform system on chip (hereinafter, the "Snapdragon SoC").  https://www.qualcomm.com/products/application/mobile-computing/laptop-device-finder/lenovo-ideapad-duet-3-chromebook

[1] The Lenovo product is charted as a representative product made used, sold, offered for sale, and/or imported by Lenovo. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)

"Integrated circuit with data communication network and IC design method"

<table>
<tr><th>'2893 Patent Claim</th><th>Lenovo Product Including Snapdragon System on Chip[1]</th></tr>
<tr><td>a plurality of functional blocks; and</td><td>The Snapdragon SoC included in the Lenovo product includes a plurality of functional blocks, for example Qualcomm Adreno GPU; Octa-core Qualcomm Kryo 468 CPU; and Qualcomm Hexagon 692 DSP:

Qualcomm® Snapdragon™
7c Gen 2 Compute Platform
Qualcomm snapdragon

Specifications & Features

CPU
• CPU Clock Speed: Up to 2.55 GHz
• CPU Cores: Octa-core Qualcomm® Kryo™ 468 CPU
• CPU Architecture: 64-bit
Process
• Process Technology: 8 nm
OS Support
• Supports Windows 10 and Windows 11
• Chrome OS
Memory
• Memory Type: 2 x 16-bit, LPDDR4x-4266
Storage
• UFS: eMMC 5.1; UFS 2.1
Visual Subsystem
• GPU: Qualcomm® Adreno™ GPU
Camera
• Image Signal Processor: Qualcomm Spectra™ 255 image signal processor, 14-bit
• Dual Camera, ZSL, 30fps: Up to 16 MP
Video
• Video Playback: Up to 4K HDR10
• Codec Support: H.265 (HEVC), H.264 (AVC), VP9
• Video Software: Motion Compensated Temporal Filtering (MCTF)
Display
• Max On-Device Display: QXGA @ 60Hz, FHD @ 60Hz
• Max External Display: QHD @ 60Hz
• Display Pixels: 2560x1440, 2048x1536
General Audio
• Qualcomm Aqstic technology: Qualcomm Aqstic™ audio codec, Qualcomm Aqstic smart speaker amplifier
• Qualcomm® aptX™ audio playback support: aptX, aptX HD
Audio Playback
• PCM, Playback: Up to 384kHz/32bit
• Additional Playback Features: Native DSD support
Qualcomm® AI Engine
• AIE CPU: Octa-core Kryo 468 CPU
• Uplink Technology: Qualcomm® Snapdragon™ Upload+
• Uplink Carrier Aggregation: 2x20 MHz carrier aggregation
• Uplink QAM: Up to 64-QAM
• LTE Speed
• LTE Peak Download Speed: 600 Mbps
Wi-Fi
• Wi-Fi Standards: 802.11ac Wave 2, 802.11a/b/g, 802.11n
• Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz
• MIMO Configuration: 2x2 (2-stream)
• Qualcomm® FastConnect™ Subsystem
Bluetooth Version
• Bluetooth 5.0
GPS Location
• Satellite Systems Support: NavIC, BeiDou, Galileo, GLONASS, GPS, QZSS, SBAS
Security
• Qualcomm® Processor Security
• Qualcomm® Content Protection
• Wi-Fi Security: WPA3</td></tr>
</table>

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

<table>
<tr><th>'2893 Patent Claim</th><th>Lenovo Product Including Snapdragon System on Chip[1]</th></tr>
<tr><td></td><td>
Camera
• Image Signal Processor: Qualcomm Spectra™ 255 image signal processor, 14-bit
• Dual Camera, ZSL, 30fps: Up to 16 MP
• Single Camera, ZSL, 30fps: Up to 32 MP
• Camera Features: Multi-frame Noise Reduction (MFNR)
• Video Capture Features: Rec. 2020 color gamut video capture, Up to 10-bit color depth video capture

CAMERA FEATURES
• Advanced DPD, WPA3
• Multi-Frame Noise Reduction (MFNR) and Multi-Frame Super Resolution (MFSR)
• Forward-looking Electronic Image Stabilization (EIS)
• Motion Compensated Temporal filtering (MCTF) for noise-free video capture up to UHD (4K) at 30 FPS
• Four MIPI CSI PHYs (DPHY 1.2 / CPHY 1.2)

• Additional Playback Features: Native DSD support

Qualcomm® AI Engine
• AIE CPU: Octa-core Kryo 468 CPU
• AIE GPU: Adreno GPU
• AIE DSP: Qualcomm® Hexagon™ 692 DSP

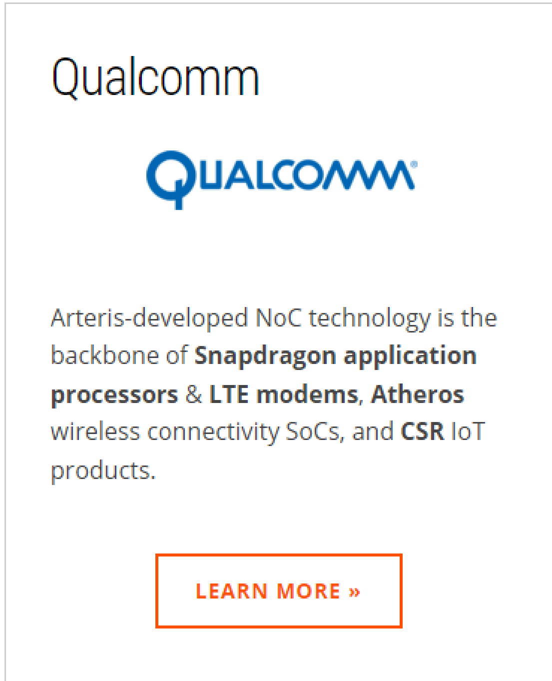
Cellular Modem
• Modem Name: Snapdragon X15 LTE modem
• LTE Category
• Downlink LTE Category: LTE Category 12
• Uplink LTE Category: LTE Category 13
• LTE Downlink Features
• Downlink Carrier Aggregation: 3x20 MHz carrier aggregation
• Downlink LTE MIMO: Up to 4x4 MIMO on two carriers
• Downlink QAM: Up to 256-QAM, Up to 64-QAM
• LTE Uplink Features

• Qualcomm® Processor Security
• Qualcomm® Content Protection
• Wi-Fi Security: WPA3

https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/prod_brief_qcom_sd7c_gen2.pdf
</td></tr>
<tr><td>a data communication network comprising a plurality of network stations being interconnected via a plurality of communication</td><td>
The Snapdragon SoC included in the Lenovo product includes a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents.

The Snapdragon SoC included in the Lenovo product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") as a data communication network:
</td></tr>
</table>

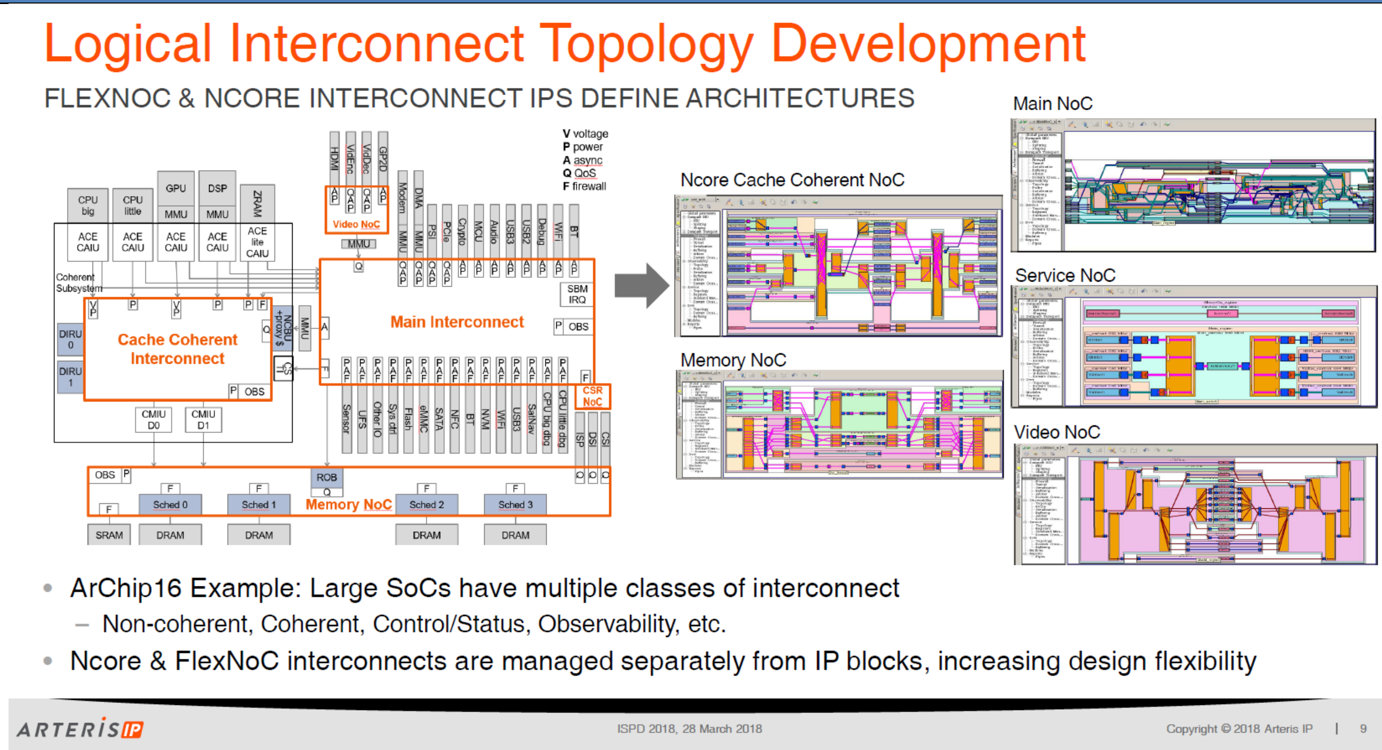
U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
channels for communicating data packages between the functional blocks,	 https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Certain Arteris Technology Assets Acquired by **Kurt Shuler**, on October 31, 2013 Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. ("Qualcomm"), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris. *Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris' Network-on-Chip interconnect IP technology.* ARTERIS IP *K. Charles Janac, President and CEO,* ***Arteris*** https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team A large SoC, such as the Snapdragon SoC included in the Lenovo product may include multiple classes of Arteris NoC data communication network:

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	

See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

The Arteris NoC in the Snapdragon SoC included in the Lenovo product is a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks.

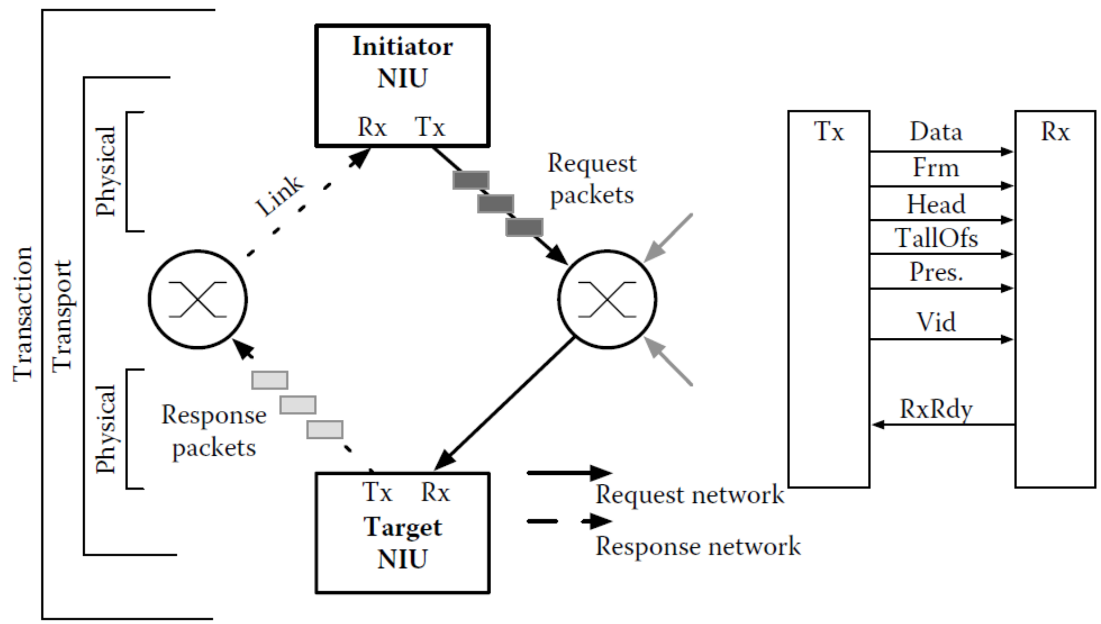
'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	For example, the Arteris NoC uses Network Interface Units (NIUs) "at the boundary of the NoC" and which "connect[] IP blocks to the network": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure."). As a further illustration, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,	In the Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, either literally or under the doctrine of equivalents. For example, the "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes": ***11.3.1.2 Transport Layer*** The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals":

4863-7801-3761.3

	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 313-314. As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information":

Field	Size	Function
Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
MstAddr	User Defined	Master address
SlvAddr	User Defined	Slave address
SlvOfs	User Defined	Slave offset
Len	User Defined	Payload length
Tag	User Defined	Tag
Prs	User defined (0 to 2)	Pressure
BE	0 or 4 bits	Byte enables
CE	1 bit	Cell error
Data	32 bits	Packet payload
Info	User Defined	Information about services supported by the NoC
Err	1 bit	Error bit

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]

StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

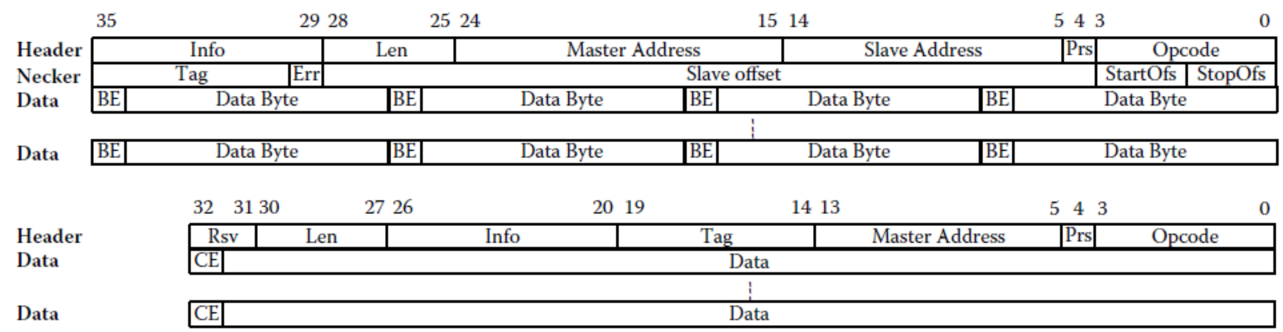


FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

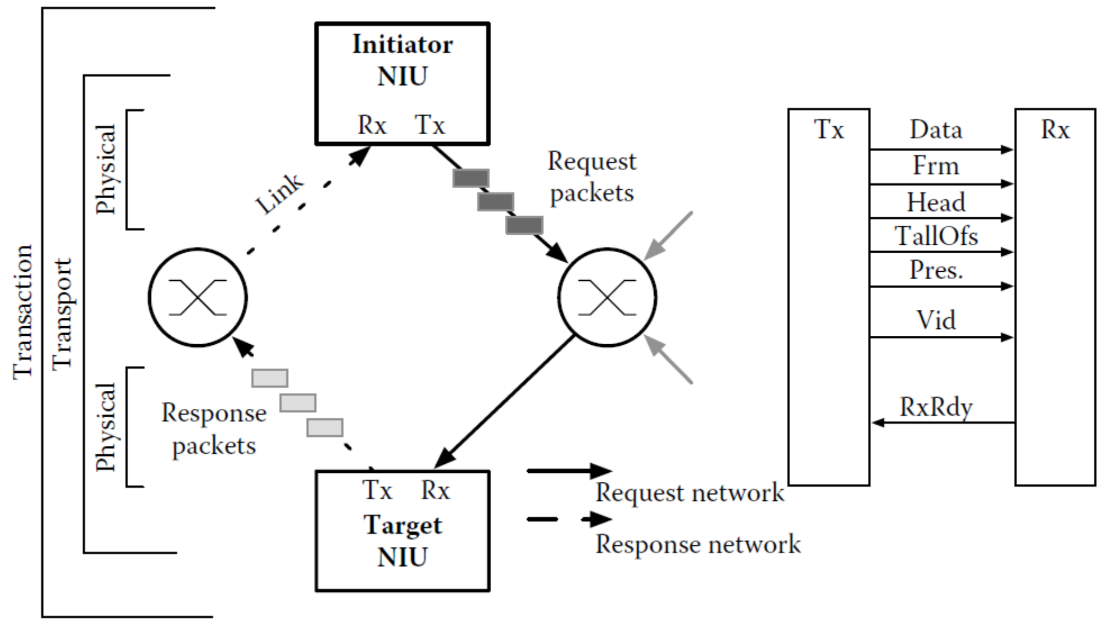
4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface,	In the Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product, the plurality of network stations comprise a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs) "at the boundary of the NoC" and which "connect[] IP blocks to the network": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. As a further illustration, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312. As a further illustration of the routers in the Arteris NoC:

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

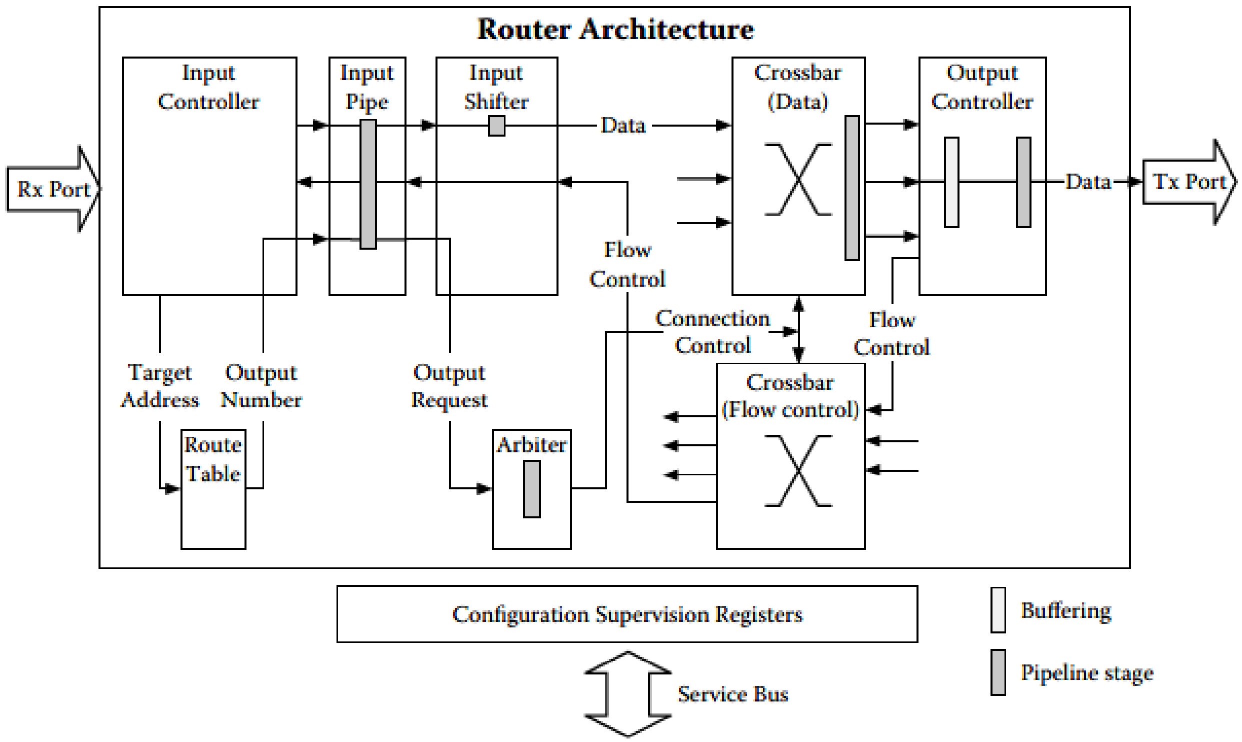


FIGURE 11.6
Packet transportation unit: Router architecture.

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	As a further illustration of the network interfaces in the Arteris NoC: ***11.3.2.1 Initiator NIU Units*** Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU. Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.

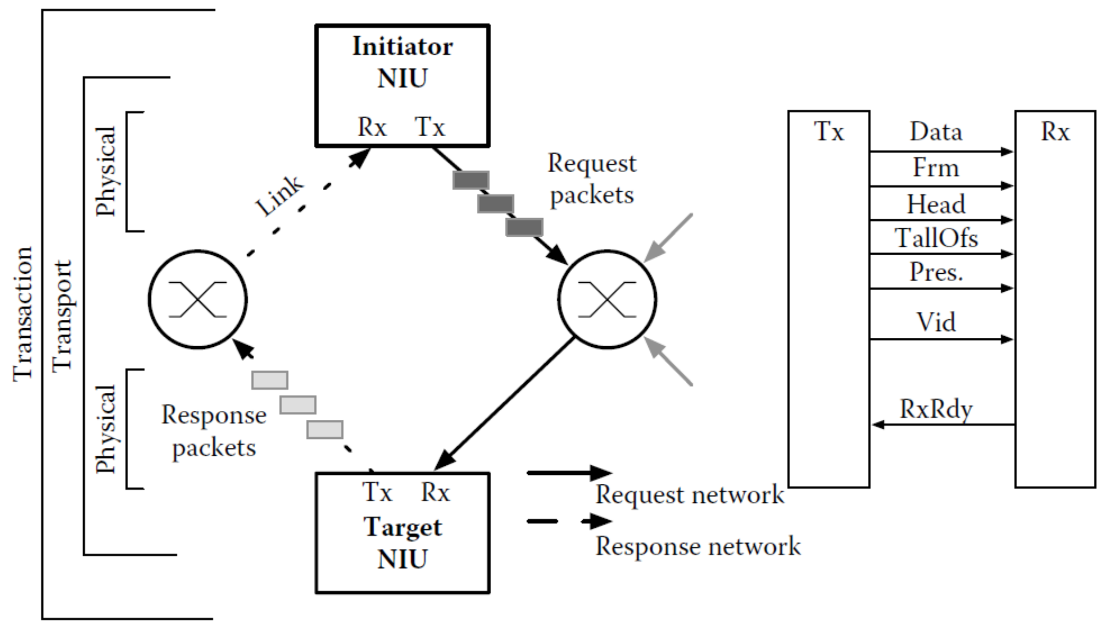
'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	11.3.2.2 Target NIU Units Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always *Id.* at 318.
the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication	In the Arteris NoC utilized in the Snapdragon SoC included in the Lenovo product, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising M*N data storage elements, M being a positive integer, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs) "at the boundary of the NoC" and which "connect[] IP blocks to the network":

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
network further comprising M*N data storage elements, M being a positive integer,	***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. As a further illustration, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

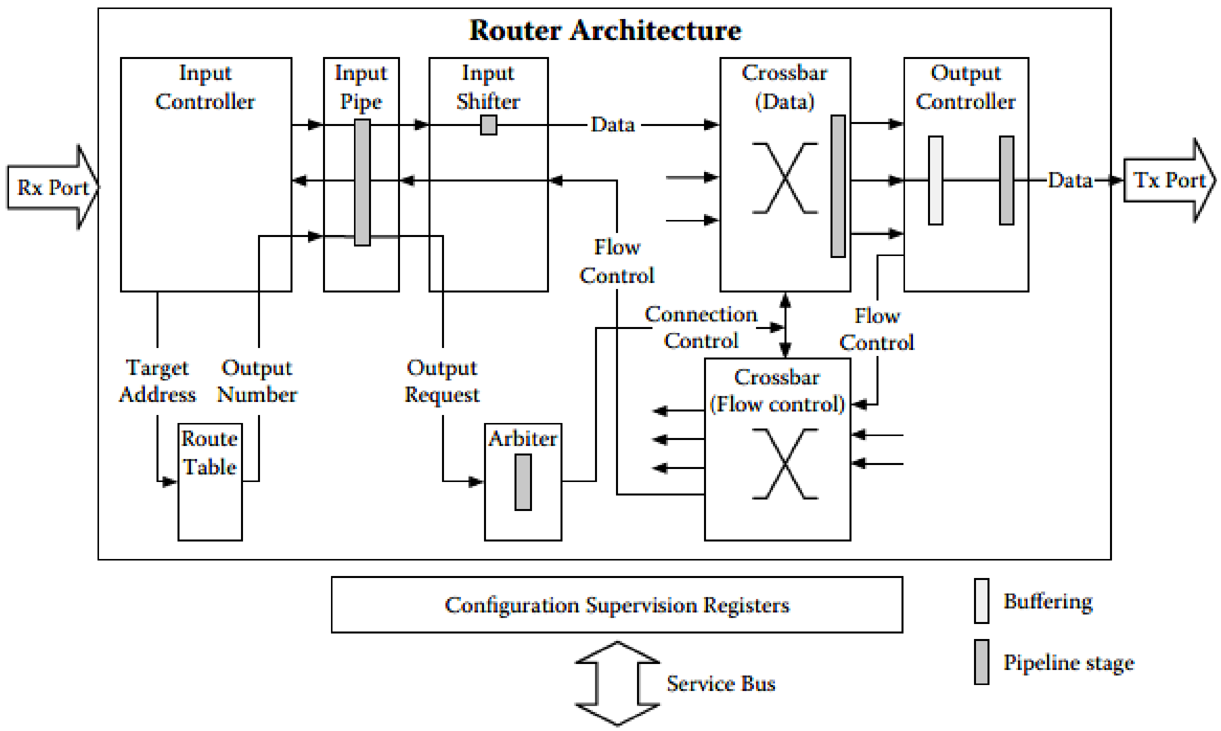
'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312. As a further example, a "delay pipeline is automatically inserted in the input controller to keep data and routing information in phase" and an input pipe "introduces a one-word-deep FIFO":

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the * * * The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322. As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element "with as many words as there are date pipelined in the crossbar":

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of *m* muxes (one per output port), each having *n* inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as *max*(*n*, *m*). The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller. *Id.* at 323. The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:

	11.3.3.2 Routing The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address  **FIGURE 11.6** Packet transportation unit: Router architecture.

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 320. As another example, the "fwdPipe" parameter "introduces a true pipeline register on the forward signals" and "inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path": get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path. *Id.* at 323-324.
the data communication introducing a delay of M*N cycles on the first communication channel when the data	In the Arteris NoC utilized in the Snapdragon SoC included in the Lenovo product, the data communication introducing a delay of M*N cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold, either literally or under the doctrine of equivalents. For example, a "delay pipeline is automatically inserted in the input controller to keep data and routing information in phase" and an input pipe "introduces a one-word-deep FIFO":

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.	Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the * * * The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322. As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element "with as many words as there are date pipelined in the crossbar":

4863-7801-3761.3

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of *m* muxes (one per output port), each having *n* inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as *max*(*n*, *m*). The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller. *Id.* at 323. The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

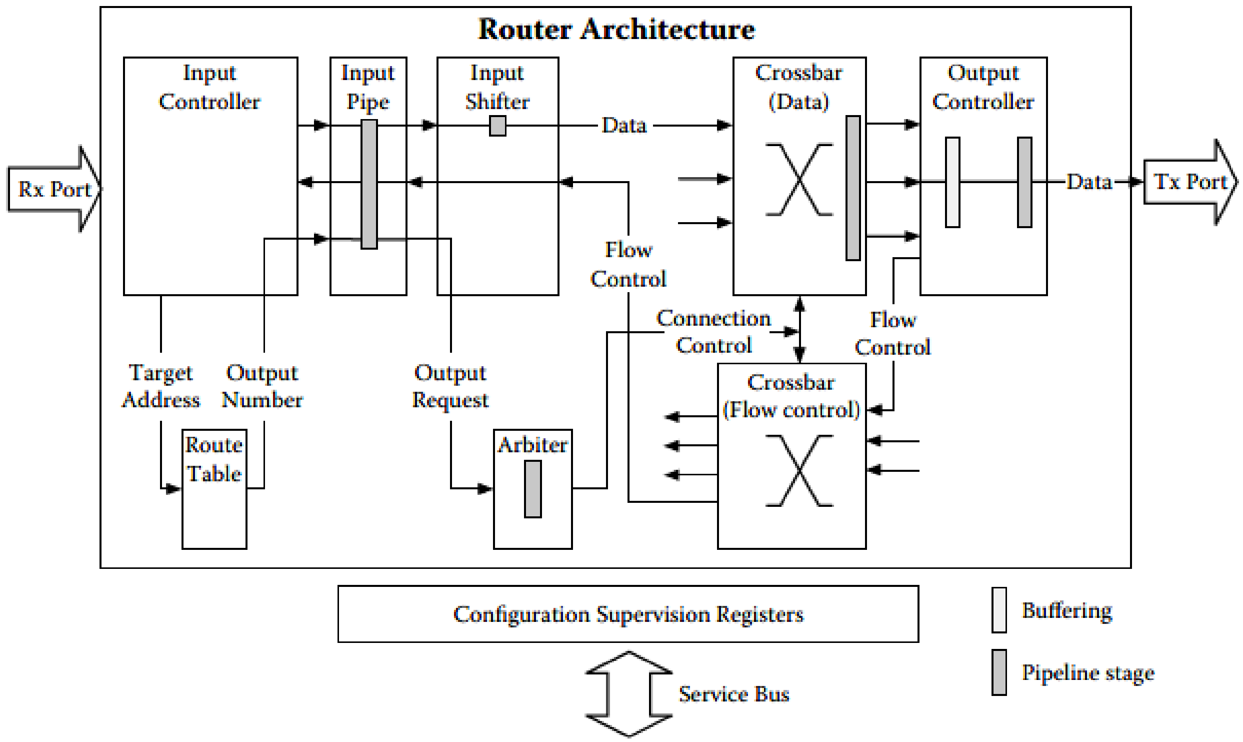


FIGURE 11.6
Packet transportation unit: Router architecture.

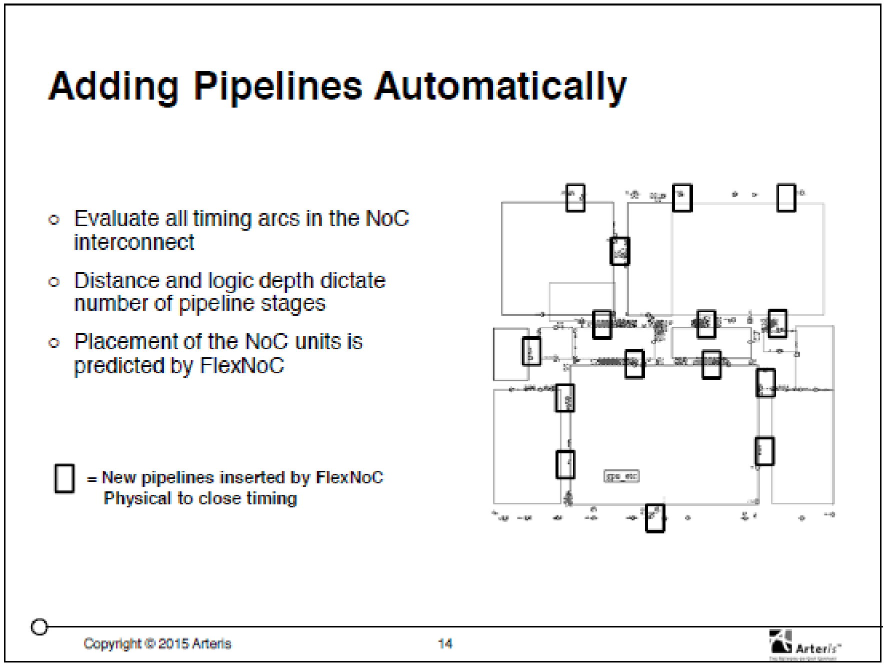
U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 320. As another example, the "fwdPipe" parameter "introduces a true pipeline register on the forward signals" and "inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path": get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path. *Id.* at 323-324. As another example, pipelines may be automatically inserted by the Arteris NoC to close timing:

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

<table>
<tr><th>'2893 Patent Claim</th><th>Lenovo Product Including Snapdragon System on Chip[1]</th></tr>
<tr><td></td><td>



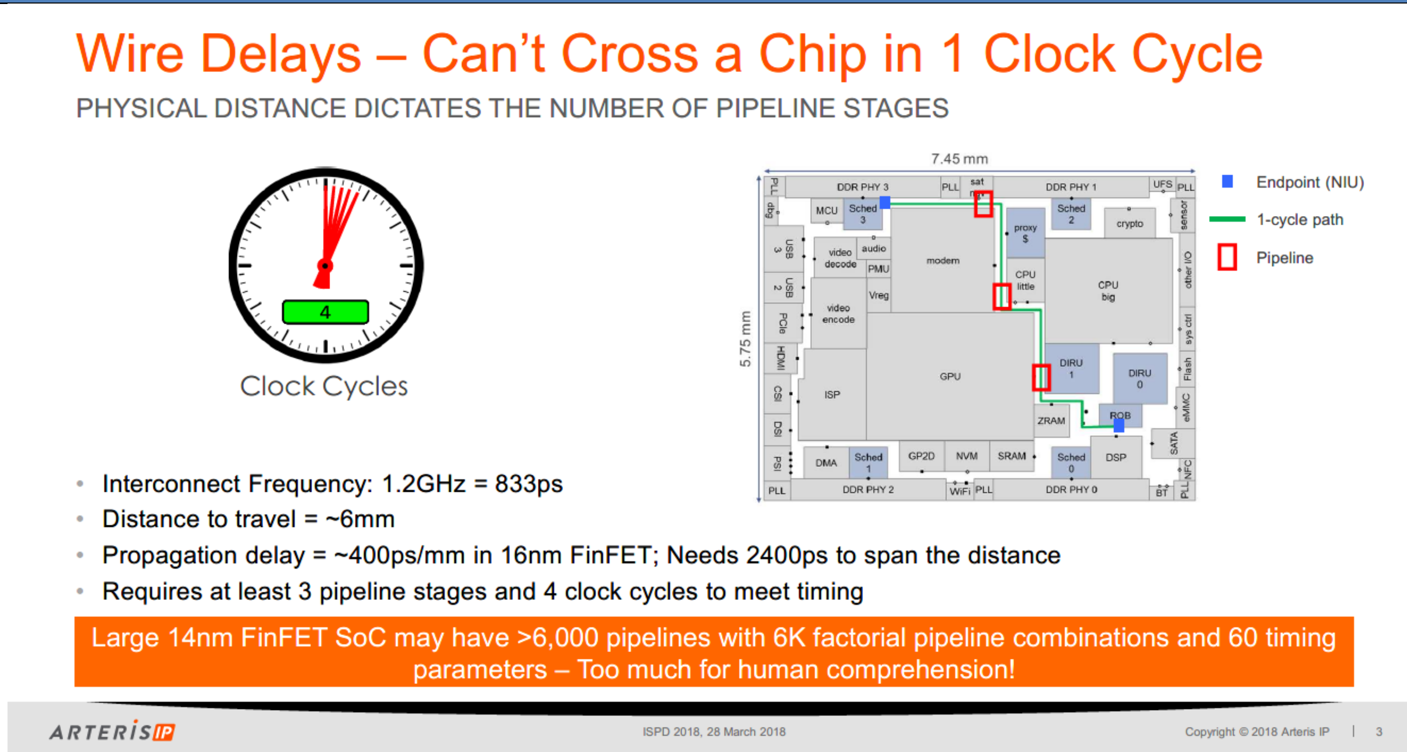
Using SoC Interconnect IPs to Improve Physical Layout, http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf, at slide 14.

As a further illustration, the Arteris NoC includes pipelining for distance spanning when traveling "~6mm" has a propagation delay of "~400ps/mm", requiring at least "2400ps to span the Distance"; thus requiring "at least 3 pipeline stages and 4 clock cycles to meet timing."

</td></tr>
</table>

4863-7801-3761.3

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.

4863-7801-3761.3